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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,470	HORIGUCHI, FUMIO	
	Examiner	Art Unit	
	Johannes P. Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 6/2/06.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 5-8,11-16,22 and 23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 22 and 23 is/are allowed.

6)☒ Claim(s) 5-8,11,12 and 14 is/are rejected.

7)☒ Claim(s) 13,15 and 16 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 23 January 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 6/6/05 forms the basis for this office action. In said Amendment Applicant substantially amended claims 5-8, 11-16 and added new claims 22 and 23. Comments on Remarks in said Amendment are provided below under "Response to Arguments".

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore,

(a) the "connection line" as claimed (as defined in lines 19-21 of claim 5) must be shown or the features canceled from the claims. No new matter should be entered.

(b) Furthermore, the second impurity layer is not shown as united with respect to adjacent three or more of the silicon columns on the bottom of the trench (as claimed, claim 15),

(c) nor is the claimed lacking pair of silicon columns at both corners on a diagonal line of the matrix form formed by the silicon columns (as claimed, claim 16) shown anywhere in the Drawings.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure

is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: the subject matter of claims 15 and 16 (original claims also in the parent) is not disclosed in the remainder of the Specification. In particular, nowhere in the Specification is the second impurity layer united with respect to adjacent three or more of the silicon columns on the bottom of the trench (claim 15), nor is there any disclosure of one pair of silicon columns lacking at both corners on a diagonal line of the matrix form formed by the plurality of silicon columns (claim 16).

Appropriate correction is required.

Claim Objections

1. ***Claim 5*** is objected to because of the following informalities: the wording "a gate insulating film formed on the channel portion, with the gate insulating film interposed therebetween" (lines 16-17) should be replaced by: "a gate insulating film formed on the

channel portion; and a gate electrode formed over the channel portion with the gate insulating film interposed therebetween". Appropriate correction is required.

2. ***Claim 22*** is objected to because of the following informalities: the wording "having two electrode" (line 19) should be replaced by: "having two electrodes". Appropriate correction is required.

3. ***Claim 23*** is objected to because of the following informalities: the wording "insulative buried" (line 25) should be replaced by: "insulatively buried". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. ***Claims 5, 7, 8, 11, 12, 14*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Goebel et al (6,172,391 B1; cf. IDS) in view of Alsmeier et al (6,201,730 B1) and Gruening et al (6,093,614).

Goebel et al teach a semiconductor memory device (title, abstract) comprising:

a silicon substrate **1a** of first conductivity type (p-type) (col. 10, l. 4) having a grid trench **G1a,** G2a, ..., (col. 10, l. 15-33) extending in two mutually orthogonal directions in an upper major surface of the silicon substrate, the trench having a width (cf. Figures 2 and 5);

a plurality of silicon columns **Ska** (col. 10, l. 4-15) formed on the major surface of the substrate and having an upper surface defined by the trench, the upper surface having a side length (cf. Figures 2, 5 and 6);

a plurality of transistors (as defined by corresponding source/drain regions S/D1a and S/D2a with channel there between in proximity to a gate: see "Summary of Invention"; see Figure 6) each formed on a side surface of the respective silicon columns, each of the transistors comprising:

a first impurity layer **S/D1a** (col. 10, l. 4-15) formed on the square upper surface of the corresponding one of the silicon columns and serving as one of a source and a drain;

a second impurity layer **S/D2a** (col. 11, l. 1-6) formed on a bottom of the trench adjacent to the corresponding one of the silicon columns and serving as the other of the source and drain;

a channel portion **Kaa** (col. 10, l. 3-15) formed on a side surface of the corresponding one of the silicon columns between the first and second impurity layers;

a gate insulating film **Gda** (col. 11, l. 60-61 and Figure 6) formed on the channel portion, and

a gate electrode **Gaa** (col. 12, l. 6) formed over the channel portion with the gate insulating film interposed therebetween;

a plurality of capacitors **P1a/Kda/P2a** (col. 12, l. 17-27) each having two electrodes **P1a** and **P2a**, one **P1a** of said two electrodes being connected to the first impurity layer (through contacts **Ka**) (col. 12, l. 11-21);

a connection line **LC** configured to bring the second impurity layer out to the major surface of the silicon substrate (col. 14, l. 14-43); and

a bit line formed **PL** above the major surface of the silicon substrate (loc.cit.), wherein the connection line LC is insulatively buried in the trench (cf. col. 14, l. 14-43 and Figure 11b) so as to extend from the second impurity layer on the bottom of the trench to an upper side of the trench and be connected to the bitline (loc.cit.).

Goebel et al do not necessarily teach the limitations of *the "square" shape* of the upper surface defined by the trench and that said connection line is also *"connected to the second impurity layer of an adjacent one of the transistors"*.

However, it would have been obvious to include the latter limitation in view of *Alsmeier et al*, who teach the bitlines to be commonly connected (see "Detailed Description", col. 2, l. 55-67). *Motivation* to include the teaching by Alsmeier et al in the invention at least derives from the savings resulting from a common bitline when the common voltage is a design aspect.

Finally, the square shape of the upper surface defined by the trench is obvious over Gruening et al, who, in a patent on vertical trench structure for memory cell arrays, hence analogous art, teach square vertical trenches (cf. col. 3, l. 14-18) on opposite sides of square bulk portions within the context of efficient utilization of chip area (see "Background of the Invention"). *Motivation* of inclusion of the teaching by Gruening et al in the invention by Goebel et al at least derives from the increased surface area available for the channel regions for square trenches in comparison with RIE trenches that are rounded.

On claim 7: in the semiconductor memory device by Goebel et al the plurality of capacitors P1a/Kda/P2a are formed on the plurality of silicon columns Ska, respectively, each of the capacitors comprising: a capacitor electrode P1a connected to the first impurity layer and the aforementioned one of the two electrodes; a dielectric film Kda formed on the capacitor electrode; and a storage electrode P2aopposite the capacitor electrode through the dielectric film (col. 12, l. 8-27).

On claim 8: each of the capacitors **P1a/Kda/P2a** has a planar size that is substantially the same as a size of the upper surface of the silicon column (cf. col. 10, l. 3-15 and Figure 6).

On claim 11: The gate electrode of the silicon columns is aligned in one direction and part of a wordline **WL**, hence are continuously connected to form a word line (cf. Figure 15 A and col. 15, l. 35-47). Also, the gate electrode **Gaa** is so formed as to surround the corresponding one of the silicon columns (cf. Figure 6, col. 11, l. 60 – col. 12, l. 6), while the connection line **LC** is formed in the trench at a central area surrounded by mutually adjacent four of the silicon columns (cf. Figures 5 and 11B) because every trench is surrounded by mutually adjacent four silicon columns.

On claims 12: The gate electrode of the silicon columns is aligned in one direction and part of a wordline **WL**, hence are continuously connected to form a word line (cf. Figure 15 A and col. 15, l. 35-47). Also, the gate electrode **Gaa** is so formed on one side surface of the silicon columns (cf. Figure 6, col. 11, l. 60 – col. 12, l. 6), while the connection line **LC** is formed in the trench along another side surface adjacent to

the one side surface, because the gate electrode is formed on both side surfaces (cf. Figures 5 and 11B).

On claim 14: The second impurity layer **S/D2a** is formed as a band configuration around the corresponding one of the silicon columns, - as forming a band embedding laterally, and surrounding the bottom portion of, the corresponding one of the silicon columns (cf. col. 11, l. 1-18).

5. ***Claim 6*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Goebel et al and Gruening et al as applied to claim 5 above, and further in view of Clampitt (6,198,158 B1). *As detailed above, claim 5 is unpatentable* over Goebel et al in view of Gruening et al. *Neither Goebel et al nor Gruening et al necessarily teach* the further limitation of claim 6. *However, it would have been obvious to include said further limitation in view of Clampitt*, who teach the widths of the silicon columns 18 and the trenches 28 to be equal in order to reduce the memory cell area (col. 4, l. 56 – col. 5, l. 3), thus meeting the claim limitation. *Motivation* for inclusion of the teaching in this regard by Clampitt in the invention by Goebel et al and Gruening et al derives at least for said reduction in memory cell area, thus enabling increased device density.

Double Patenting

6. ***Claim 13*** is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 22. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

7. ***Claim 15*** is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 23. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Response to Arguments

1. Applicant's arguments filed 6/6/05 have been fully considered but they are, on the whole, not persuasive.

2. With regard to the claim objections for minor informalities and the rejections under 35 U.S.C. 112, second paragraph, Applicant's amendment has overcome said objections and rejections by said Amendment.

3. With regard to the response in said Remarks in traverse of the objections to the Specification and the Drawings,

(a) Applicant incorrectly identifies the "connection line" "configured to bring the second impurity layer" "out to the major surface of the silicon substrate" (lines 20-22 of claim 5) with the component or element of reference number 128, because 128 is connected to the first and not to the second impurity layer, the "second impurity layer" being "formed on a bottom of the trench" (see lines 12-13). Therefore, the objection to the Drawings ad (a) stands.

(b) Furthermore, the reference to Fig. 56 and to the fifth embodiment, page 34, line 3, to page 35, line 7 is not persuasive because Fig. 56 in it self fails to show, - and the remainder of Specification fails to teach, an electrical connection between 201 and

202 while reference is made to Figures 5 and Figures 45A and 45B, none of which even show either element 201 or element 202, nor do any of the Figures show the second impurity layer (i.e., the one at the bottom of the trench) "united with respect to adjacent three or more of the silicon columns on the bottom of the trench" as recited in claim 15. Therefore, the objections to the Specification and the Drawings ad (b) stand.

(c) Also, while Fig. 57 show silicon columns lacking at corners of a matrix form said lacking silicon columns are not lacking at corners on a *diagonal line of the matrix form*, said diagonal line being absent in view of the even rank of the matrix shown. Therefore, the objections to the Specification and the Drawings ad (c) stand.

4. Applicant's arguments on the rejections under 35 U.S.C. 103(a) are also not persuasive, because a verbatim recitation that LC is connected with SD2, i.e., source/drain regions on the bottom of the trench is found in the very passage as cited in the previous office action, i.e., particularly col. 14, l. 14-43 and more specifically: col. 14, l. 26-29. Accordingly, the rejections under 35 U.S.C. 103(a) stand.

Allowable Subject Matter

5. ***Claims 13, 15 and 16*** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: within the context of the semiconductor memory device according to claim 5 the further limitations defined by claims 13, 15 and 16 are not taught by Goebel et al. No prior art has been found.

6. ***Claim 22*** is allowed. The following is a statement of reasons for the indication of allowable subject matter: within the context of the semiconductor memory device defined by claim 5 the further limitation as defined by claim 13 and written in independent form as claim 22 (see objection under "Double Patenting" to claim 13) is not taught by Goebel et al. No prior art has been found.

7. ***Claim 23*** is allowed. The following is a statement of reasons for the indication of allowable subject matter: within the context of the semiconductor memory device defined by claim 5 the further limitation defined by claim 15 and written in independent form as claim 23 (see objection under "Double Patenting" to claim 15) is not taught by Goebel et al. No prior art has been found.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
August 14, 2005

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